WHAT IS CLAIMED IS:

1. An averaging circuit comprising:

input signal nodes for providing input signals;

a multiplexing circuit coupled to the input signal nodes for switching between the input signals to create a time waveform;

a low pass filter coupled to an output of the multiplexing circuit for filtering the time waveform to create an average signal; and

an average replication circuit coupled to an output of the low pass filter.

2. The circuit of claim 1 wherein the multiplexing circuit comprises a switch bank coupled to the input signal nodes.

3. The circuit of claim 1 wherein the low pass filter comprises an RC circuit.

4. The circuit of claim 2 wherein the low pass filter comprises an RC circuit.

5. The circuit of claim 3 wherein the RC circuit comprises a resistor coupled in parallel with a capacitor.

6. The circuit of claim 4 wherein the RC circuit comprises a resistor coupled in parallel with a capacitor.

7. The circuit of claim 1 wherein the average replication circuit comprises:

an amplifier having a first input coupled to the output of the low pass filter;

a transistor having a control node coupled to an output of the amplifier and a non-control node coupled to a second input of the amplifier; and

a resistor coupled to the second input of the amplifier.

8. The circuit of claim 5 wherein the average replication circuit comprises:

an amplifier having a first input coupled to the resistor;

a transistor having a control node coupled to an output of the amplifier and a non-control node coupled to a second input of the amplifier; and

a replication resistor coupled to the second input of the amplifier.

9. The circuit of claim 8 wherein the resistor and the replication resistor are matched.

10. The circuit of claim 1 wherein the multiplexing circuit randomly selects the input signal nodes.

11. The circuit of claim 1 wherein the multiplexing circuit sequentially selects the input signal nodes.

12. The circuit of claim 1 wherein the low pass filter comprises:

a transistor coupled to the output of the multiplexing circuit; and

a capacitor coupled to a control node of the transistor and to the output of the multiplexing circuit.

13. The circuit of claim 1 wherein the average replication circuit comprises a transistor having a control node coupled to the low pass filter.

14. The circuit of claim 12 wherein the average replication circuit comprises a replication transistor having a control node

coupled to the capacitor.

15. The circuit of claim 14 wherein the transistor and the replication circuit are matched.

16. The circuit of claim 12 wherein the average replication circuit comprises:

a first switch coupled between the multiplexing circuit and the control node of the transistor; and

a second switch coupled between the multiplexing circuit and an output node.